We Claim:

1. A method for amplitude trimming between an analog modulation signal and a digital modulation signal for a PLL circuit operating based on a two-point modulation, the method which comprises:

locking the PLL circuit onto a desired carrier frequency without impressing any modulation;

impressing the analog modulation signal into the PLL circuit, which is locked, via a summation point connected to an input of a voltage-controlled oscillator and impressing the digital modulation signal into a frequency divider configured in a feedback path of the PLL circuit resulting in a PLL control error;

obtaining a signal that is characteristic of the PLL control error from the PLL circuit; and

changing a modulation swing in the analog modulation signal such that the signal that is characteristic of the PLL control error has a value that is the same as a value of the signal that is characteristic of the PLL control error before the analog modulation signal and the digital modulation signal were impressed.

2. The method according to claim 1, wherein the signal that is characteristic of the PLL control error in the PLL circuit is a voltage signal obtained from the PLL circuit via a charge pump and a low-pass filter.

3. The method according to claim 1, which further comprises:

obtaining a comparison signal by comparing the signal that is characteristic of the PLL control error with a reference signal having a fixed value;

obtaining an evaluation result by evaluating the comparison signal before and after performing the step of impressing the analog modulation signal and the digital modulation signal; and

performing the step of changing the modulation swing in the analog modulation signal based on the evaluation result.

4. The method according to claim 3, which comprises obtaining the reference signal by:

adjusting the PLL circuit in a deactivated state to a desired channel center frequency;

activating the PLL circuit and thereby locking the PLL circuit; and

producing the reference signal from the signal that is characteristic of a control error in the PLL circuit while the PLL circuit is being locked.

5. The method according to claim 3, wherein the reference signal is a prescribed external reference signal.

6. A PLL circuit designed for impressing an analog modulation signal and a digital modulation signal based on a two-point modulation, the circuit comprising:

a summation point having an output and an input for obtaining the analog modulation signal;

a voltage-controlled oscillator having an input connected to said output of said summation point;

a feedback path;

a frequency divider configured in said feedback path, said frequency divider obtaining the digital modulation signal; and

an associated trimming device including:

a device for tapping a signal being characteristic of a PLL control error arising when the analog modulation signal and the digital modulation signal are impressed,

a device for obtaining an evaluation result by evaluating the signal being characteristic of a PLL control error, and

a device for changing a modulation swing in the analog modulation signal based the evaluation result.

7. The PLL circuit according to claim 6, wherein said device for tapping the signal being characteristic of the PLL control error includes a charge pump and a low-pass filter connected downstream from said charge pump.

8. The PLL circuit according to claim 6, wherein said device for obtaining an evaluation result by evaluating the signal being characteristic of a PLL control error includes:

a device for comparing the signal being characteristic of the control error with a reference signal having a fixed value, thus producing a comparison signal, and

a device for evaluating the comparison signal before and after the analog modulation signal and the digital modulation signal are impressed.

9. The PLL circuit according to claim 8, further comprising a switching device configured such that said device for tapping the signal being characteristic of the PLL control error produces the reference signal during a locking process in the PLL circuit.